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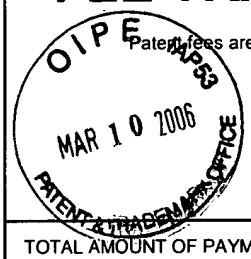

TOTAL AMOUNT OF PAYMENT ($) 180.00

Complete If Known	
Application Number	10/766,564
Filing Date	29 January 2004
First Named Inventor	TAE-SUNG KIM
Examiner Name	ERDEM, FAZLI
Group/Art Unit	2826
Attorney Docket No.	P57001

METHOD OF PAYMENT (check one)

1. ■ **Payment Enclosed: (CHECK #50537)**
   ■ Check ❑ Credit Card ❑ Money Order
   ❑ Other

❑ Charge Any Additional Fee Required Under 37 C.F.R. §1.16 and 1.17.

❑ Applicant claims small entity status. See 37 CFR 1.27

2. ■ The Commissioner is hereby authorized to charge any deficiency and credit any over payments to:

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FEE CALCULATION

Fee Code	Fee ($)	Fee Code	Fee ($)	Fee Description	Fee Paid
				EXTENSION OF TIME FEES	
1251	120	2251	60	Extension for reply within first month	$
1252	450	2252	225	Extension for reply within second month	$
1253	1020	2253	510	Extension for reply within third month	$
1254	1590	2254	795	Extension for reply within fourth month	$
1255	2160	2255	1080	Extension for reply within fifth month	$
				APPEAL	
1401	500	2401	250	Notice of Appeal	$
1402	500	2402	250	Filing a brief in support of an appeal	$
1403	1000	2403	500	Request for oral hearing	$
				CLAIMS	
1201	200	2201	100	Independent claims in excess of 3	$
1202	50	2202	25	claims in excess of 20	$
Other Fee (specify)					$
Other Fee (specify)					$
Other Fee (specify)					$

FEE CALCULATION

Fee Code	Fee ($)	Fee Code	Fee ($)	Fee Description	Fee Paid
				MISCELLANEOUS	
1801	$790	2801	$395	Request for continued examination (RCE)	$
1806	$180			Submission of an IDS	$180.00
1814	$130	2814	$65	Statutory disclaimer	$
8021	$40			Recordation of assignment per property	$
				TRADEMARK	
6001/7001			$335	Application for registration, per class	$
6002/7002			$100	Amendment to Allege Use, per class	$
6003/7003			$100	Statement of Use, per class	$
6004/7004			$150	Request for six-month extension of time, per class	$
6205/7205			$100	§8 affidavit, per class	$
6208/7208			$200	§15 affidavit, per class	$
6201/7201			$400	Application for renewal, per class	$
6403/7403			$100	Ex parte appeal, per class	$
				PETITION	
1462			$400	Petitions to Director (Group I)	$
1463			$200	Petitions to Director (Group I)	$
1464			$130	Petitions to Director (Group II)	$
1452	$500	2452	$250	Petitions to revive unavoidably abandoned application	$
1453	$1500	2453	$750	Petitions to revive unintentionally abandoned application	$
				PATENT MAINTENANCE	
1551	$900	2551	$450	Due at 3.5 years	$
1552	$2300	2552	$1150	Due at 7.5 years	$
1553	$3800	2553	$1900	Due at 11.5 years	$
Other Fee (specify)					$
Other Fee (specify)					$
Other Fee (specify)					$

SUBTOTAL: LEFT COLUMN	$ 0.00	SUBTOTAL: RIGHT COLUMN	$ 180.00

SUBMITTED BY

Typed or Printed Name	Robert E. Bushnell, Esq.	Reg. Number	27,774
Signature	/Robert E. Bushnell/	Date: 10 March 2006	Deposit Account User ID:

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAE-SUNG KIM

Serial No.:	10/766,564	Examiner:	ERDEM, FAZLI
Filed:	29 January 2004	Art Unit:	2826

For: NOVEL CONDUCTIVE ELEMENTS FOR THIN FILM TRANSISTORS USED IN A FLAT PANEL DISPLAY

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97 and 1.98 as amended, Applicant cites, describes, and provides copies of the following art references. Under 37 C.F.R. §1.98(a)(2) however, copies of U.S. patent reference(s) are not provided.

US PATENT REFERENCE:

- United States Patent No. 6,414,738 to Fujikawa, entitled *DISPLAY*, issued on 2 July 2002.
- United States Patent No. 5,747,879 to Rastogi, *et al.*, entitled *INTERFACE BETWEEN TITANIUM AND ALUMINUM-ALLOY IN METAL STACK FOR INTEGRATED CIRCUIT*, issued on 5 May 1998.
- United States Patent No. 6,255,706 to Watanabe, *et al.*, entitled *THIN FILM TRANSISTOR AND METHOD OF MANUFACTURING SAME*, issued on 3 July 2001

- United States Patent Application No. 2001/0043175 to Yasukawa, entitled *LIQUID*

CRYSTAL PANEL SUBSTRATE, LIQUID CRYSTAL PANEL, AND ELECTRONIC EQUIPMENT AND PROJECTION TYPE DISPLAY DEVICE BOTH USING THE SAME, issued on 22 November 2001.

- United States Patent Application No. 2002/0076574 to Cabral, Jr., *et al.*, entitled *INTERCONNECTS WITH TI-CONTAINING LINERS*, issued on 20 January 2002.
- United States Patent Application No. 2002/0085157 to Tanaka, *et al.*, entitled *ACTIVE MATRIX ADDRESSING LIQUID-CRYSTAL DISPLAY DEVICE*, issued on 4 July 2002.

FOREIGN PATENT REFERENCE:

- European Patent Publication No. 1001463 to Cichy, *et al.*, entitled *ALUMINUM INTERCONNECTS FOR INTEGRATED CIRCUITS COMPRISING TITANIUM UNDER AND OVERLAYERS*, published on 17 May 2000 (with English abstract).

OTHER DOCUMENTS:

- European Office action for European Patent Application No. 04250453.0, issued on 30 January 2006.
- An article "Relationship between copper concentration and stress during electromigration in an Al(0.25 at. % Cu) conductor line" written by Kao, *et al.* published in Journal of Applied Physics, Vol. 93, no. 5, pp 2516-2527, on 1 March 2003 (with English abstract).
- An article "The microstructure of submicrometer wide planar-reactive ion etched versus trench-damascene AlCu lines: written by Rodbell, *et al.*, published in Journal of Applied Physics, Vol. 88, no. 9, pp 5093-5099, on 1 November 2000 (with English abstract).
- An article "Stress Induced Metallurgical Effects in Ti/TiN/AlCu/TiN Metal Stacks" written by Koller, *et al.*, published in Stress Induced Phenomena in Metallization,

Vol. 612, pp 235-246, on April 2002 (with English abstract).

DISCUSSION

Fujikawa US'738, according to the European Office action in applicant's European patent application Serial No. 04250453.0, discloses that in a display device such as a liquid crystal display device, in order to connect electrodes and wiring with a low resistance, the first titanium nitride film having a hexagonal crystal structure for preventing silicon diffusion is intervened between the drain region composed of a polycrystalline silicon film and the drain electrode composed of an aluminum film. the second titanium nitride film having a hexagonal crystal structure which can be deposited by sputtering with the same target as that for the titanium film and the first titanium film is intervened between the transparent display electrode composed of an ITO film and the drain electrode composed of an aluminum film in order to bring them into ohmic contact. Since the second titanium nitride film is resistant to an etchant for the silicon oxide film and to an etchant for the ITO film, the drain electrode is protected when etching is performed.

Rastogi US'879, discloses that an improvement in a metal stack used for interconnecting structures in an integrated circuit. The improvement comprises the entrapping in a titanium layer of nitrogen at the interface where the titanium layer contacts a bulk conductor layer such as an aluminum-copper alloy layer. The entrapped nitrogen prevents the formation of any substantial amount of titanium aluminide thereby reducing current densities and also improving the electromigration properties of the stack. As currently preferred, the nitrogen is entrapped in approximately the first 30Å of the titanium layer.

Watanabe US'706, discloses that a thin film transistor wherein at least one of a gate electrode and/or a scanning line therefor and source/drain electrode and/or signal lines therefor comprises a laminated wiring structure in which a main wiring layer formed of a metal selected from

Al and Cu or an alloy based on the metal is sandwiched between an underlying wiring layer and an overlayer, the underlying and overlaying wiring layers being formed of a material based on a metal or alloy of metals and containing nitrogen, the metal being selected from Ti, Mo, W, Cr, Al and Cu, and the materials used in the underlying and overlaying wiring layers being different from each other. Alternatively, the underlying and overlaying wiring layers are formed of a material based on the same metal or alloy of metals and containing nitrogen, the metal being selected from Ti, No, W, Cr, Al and Cu, and contents of nitrogen in the underlying and overlaying wiring layers being different from each other. A method of manufacturing such a thin fil, transistor is also disclosed.

Yasukawa US'175, discloses that the present invention is a liquid crystal panel substrate that comprises; pixel units each having a pixel electrode, to be used as a reflective electrode and arranged in a matrix pattern on a substrate, and a switching element controlling a voltage applied to the pixel electrode; wherein between the pixel electrode and a conductive layer forming a terminal electrode of the switching element, a contact hole is provided for connecting the pixel electrode and the terminal electrode. A light-shielding layer, having an opening surrounding the portion in which the contact hole is formed, and having no opening in regions between a plurality of adjacent pixel electrodes, is formed between the pixel electrode and the conductive layer. Harmful effects due to light leaking through a space between the pixel electrodes can thereby be prevented.

Cabral US'574, discloses that an electrical conductor for use in an electronic structure is disclosed which includes a conductor body that is formed of an alloy including between about 0.001 atomic % and about 2 atomic % of an element selected from the group consisting of Ti, Zr, In, Sn and Hf; and a liner abutting the conductor body which is formed of an alloy that includes Ta, W, Ti, Nb and V. The invention further discloses a liner for use in a semiconductor interconnect that is formed of a material selected from the group consisting o f Ti, Hf, In, Sn, Zr and alloys thereof, $TiCu_3$, $Ta_{1-X}Ti_X$, $Ta_{1-X}Hf_X$, $Ta_{1-X}In_{XY}$, $Ta_{1-X}Sn_X$, $Ta_{1-X}Zr_X$.

Tanaka US'157, discloses that an active matrix addressing LDC device having an active matrix substrate on which conductive lines are formed is provided, which suppress the Al hillock without complicating the structure of the lines and which decreases the electrical connection resistance increase at the terminals of the lines, thereby improving the connection reliability. The device comprises an active matrix substrate having a transparent, dielectric plate, thin-film transistors (TFTs) arranged on the plate, and pixel electrodes arranged on the plate. Gate electrodes of the TFTs and scan lines have a first multilevel conductive structure. Common electrodes and common lines may have the first multilevel conductive structure. Source and drain electrodes of the TFTs and signal lines may have a second multilevel conductive structure. Each of the first and second multilevel conductive structures includes a three-level TiN/Ti/Al or TiN/Al/Ti structure or a four-level TiN/Ti/Al/Ti sturucture. Each of the TiN film of the first and second structures has a nitrogen concentration of 25 atomic % or higher. The Al film may be replaced with an Al alloy.

Cichy EP'463, discloses that an interconnect for an integrated circuit includes an underlayer comprising titanium having reduced contamination for improved electromigration and for supporting another layer. An intermediate layer comprising aluminum is deposited over the underlayer. An overlayer comprising titanium having increased contamination relative to the underlayer to provide a reduced sheet resistance is applied over the intermediate layer. The resulting interconnect has improved reliability and functionality. A method is also provided.

Kao, discloses that synchrotron-based x-ray microbeam fluorescence and diffraction have been used for *in situ* measurements of Cu concentration and biaxial stress in a 200-μm-long, 10-μm-wide Al(0.25 at. % Cu) conductor line with 1.5-μm-thick SiO_2 passivation during electromigration. Measurements over 48 h with T=300°C and j=1.5x10^5 A/cm^2 show that a stress gradient of 3 MPa/μm develops over the upstream 130 μm of line length where Cu concentration drops below 0.15 at. %, and a 10-μm-long void develops at the cathode end of the line, but little change in stress occurs over the downstream 70 μm of line length where Cu concentration remains above 0.15 at. %. These experimental results have been reproduced by a finite element model in which the downstream Cu transport is accompanied by a counter flow of Al in the upstream direction, and downstream Al

motion is clocked where the local Cu concentration is above ~0.15 at. %. Defect mediated coupling between Al and Cu diffusive flows, e.g., Cu-vacancy binding, is proposed as the cause for the counterflow of Al when the Cu concentration is above the critical concentration, and as the mechanism by which Cu reduces the rate of electromigration damage in Al(Cu) conductor lines.

Rodbell, discloses that the microstructure was measured for AlCu lines, formed using either a traditional planar metal subtractive etch process or a newly developed hot AlCu-trench-damascene process. It was found that 0.35 μm wide damascene AlCu lines formed a large grained bamboo microstructure with little or no Al (lll) texture. The local crystallographic texture was measured in a scanning electron microscope using electron backscatter pattern analysis often referred to as backscatter Kikuchi diffraction. Damascene structures consisted of AlCu films deposited at greater than 400°C onto Ti or Ti/TiN into preformed amorphous SiO_2 trenches, 0.3-5.0 μm wide by 0.4 μm deep, followed by aluminum chemical mechanical polishing to remove the metal overburden. Standard planar metal control samples consisted of blanket Al or AlCu films deposited onto either an amorphous SiO_2 substrate or onto SiO_2/Ti/TiN substrates, followed by subtractive etching to define 0.45-10 μm wide lines as well as large (e.g. 10x10 μm^2) pads. The planar metal samples exhibited either little change or a slight strengthening of their (lll) fiber texture with decreasing line width; this was in sharp contrast to the damascene films in which a marked weakening in the (lll) fiber texture with decreasing line width was found. In addition a trimodal (lll) texture distribution developed in trenches where $TiAl_3$ intermetallic formed. the role of intermetallic formation ($TiAl_3$), elevated (>400°C) AlCu deposition temperature, large bamboo grain size, local AlCu crystallographic texture and differences in sidewall coverage between subtractive etched and trench-damascene processed AlCu on film microstructure are examined.

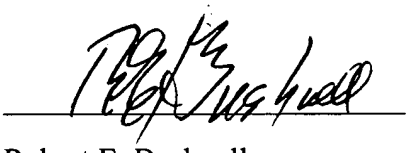
Koller, discloses that integrated circuits with aluminum metallization for products with high current densities need a metal stack with liner and antireflective coating (ARC) which ca fulfill several requirements (e.g. low sheet resistance, high reliability, smooth surface, good adhesion, thermal stability, etc.). In this work different multilayer metal stacks are investigated and several phenomena which can be observed after thermal annealing of Ti/TiN/AlCu/TiN stacks are described and discussed. Metallurgical, electrical and mechanical properties of different layer combinations are investigated after thermal annealing and stress tests are done to compare the electromigration and life time behaviour of each metal stack. For all investigated metal stacks it is shown that an interface reaction between Ti and aluminum will form $TiAl_3$ phase. Even with very thick TiN layers on top of titanium or with only TiN liner the phase formation occurred. Explanations and models for the formation of different phenomena (hillocks, depressions and elevations), are discussed. The origin of each phenomena is stress related and assisted either by the liner material and/or the ARC layer. A qualitative model which explains the different observed layer reactions is discussed.

Pursuant to 37 CFR §1.97(d), the undersigned attorney hereby certifies that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign patent application not more than three (3) months prior to the filing of the statement.

The citation of the foregoing references is not intended to constitute an assertion that other or more relevant art does not exist. Accordingly, the Examiner is requested to make a wide-ranging and thorough search of the relevant art.

Pursuant to 37 C.F.R. §1.97(c)(2), the fee set forth under 37 C.F.R.§1.17(p) of $180.00 accompanies this Information Disclosure Statement. Should the check become lost, be deficient in payment, or should other fees be incurred, the Commissioner is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,



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INFORMATION DISCLOSURE STATEMENT PTO-1449 (PAGE 1 OF 1)	SERIAL NUMBER 10/766,564	DOCKET NO. P57001
	APPLICANT TAE-SUNG KIM	
	FILING DATE 29 January 2004	GROUP 2826

U.S. PATENT DOCUMENTS

EXAMINER	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,414,738	07/02	*Fujikawa*			
	5,747,879	05/98	*Rastogi, et al.*			
	6,255,706	07/01	*Watanabe, et al.*			
	2001/0043175	11/01	*Yasukawa*			
	2002/0076574	06/02	*Cabral, Jr., et al.*			
	2002/0085157	07/02	*Tanaka, et al.*			

FOREIGN PATENT DOCUMENTS						TRANSLATION	
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	YES	NO
	EP 1 011 463	05/00	EUROPE			Abstract	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	European Office Action of the European Patent Application No. 04250453.0, mailed on 30 January 2006
	An article "Relationship between copper concentration and stress during electromigration in an Al(0.25 at. % Cu) conductor line" written by Kao, *et al.* published in Journal of Applied Physics, Vol. 93, no. 5, pp 2516-2527, on 1 March 2003.
	An article "The microstructure of submicrometer wide planar-reactive ion etched versus trench-damascene AlCu lines: written by Rodbell, *et al.*, published in Journal of Applied Physics, Vol. 88, no. 9, pp 5093-5099, on 1 November 2000.
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EXAMINER:	*DATE CONSIDERED:*

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.